**Simulation Result**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| size | Adders | Delay(ps) | Area(µm2) | Power(nw) | | |
|  |  |  |  | Leakage | Switching | Total |
| 32 | 4\*8  CSLA  Proposed | 2361  2296 | 2430  1851 | 171.651  132.482 | 124792.166  88065.675 | 124963.817  88198.15 |
| 2\*1+5\*6  CSLA  Proposed | 2354  2176 | 2553  1943 | 181.329  139.725 | 121886.088  92739.341 | 122067.417  92879.087 |
| 2\*1+3\*2+4\*1+5\*4  CSLA  Proposed | 2296  2135 | 2638  1880 | 186.874  134.750 | 129395.039  89905.130 | 129581.913  90039.880 |

**Output Values**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| size | Adders | Delay(ps) | Area(µm2) | Power(nw) | | |
|  |  |  |  | Leakage | Switching | Total |
| **64** | **4\*16**  CSLA  Proposed | 4398  2296 | 5207  1851 | 368.123  132.482 | 264767.662  88065.675 | 266165.662  88198.15 |
| **2\*1+3\*2+4\*1+5\*10**  CSLA  Proposed | 4029  3296 | 5271  3823 | 374.281  274.351 | 258319.732  177981.658 | 258694.013  178256.009 |